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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/826,003 | 04/16/2004 | Shih-Chang Shei | JCLA12118 | 9227 |

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| EXAMINER | |
|---|---|
| ANDUJAR, LEONARDO | |
| ART UNIT | PAPER NUMBER |
| 2826 | |
| MAIL DATE | DELIVERY MODE |
| 03/21/2008 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/826,003 | SHEI ET AL. | |
| | Examiner | Art Unit | |
| | Leonardo Andújar | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *9-12,14 and 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-12, 14 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/19/2007 has been entered.

### *Election/Restrictions*

2. Applicant's election without traverse of species II (fig. 3 & claims 7-15) in the reply filed on 01/23/2007 is acknowledged.

### *Claim Rejections - 35 USC § 103*

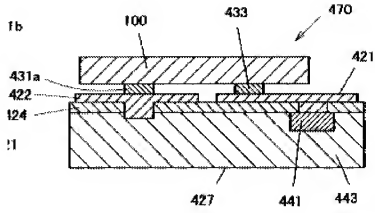
3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

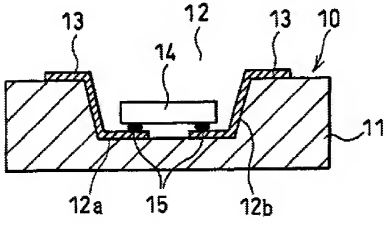
4. Claims 7-12, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano et al. (US 6,445,0011) in view of Tominaga (US 2002/0008325) further in view of Okazaki et al. (US 5,298,768).

5. Regarding claim 7, Hirano (e.g.11A & 11B, col. 3/lls. 58-61) teaches most aspects of the instant invention including a light-emitting diode package structure, comprising: a semiconductor sub-mount having a first surface, a first conductive type

semiconductor 443 and second type region 441 enclosed by the first conductive type semiconductor substrate; an insulating layer 424 set up on the first conductive type semiconductor substrate; a first patterned conductive-reflective film 422 set up on a portion of the first surface in order to directly cover part of the first conductive type semiconductor substrate; a second patterned conductive-reflective film 421 set up on a portion of the first surface and separated from the first conductive type semiconductor by the insulating layer, and a light-emitting diode chip 100 set up on the semiconductor sub-mount, wherein the light-emitting diode has a first electrode (e.g. electrode connected to 433) and a second electrode (e.g. electrode connected to 431a) electrically connected to the first patterned conductive-reflective film and the second patterned conductive-reflective film but does not disclose that the first surface has a cavity having a first sidewall, a bottom surface, and a second sidewall. Therefore, Hirano does not teach that the first pattern is set up on a portion of the first sidewall, bottom surface that the second portion is set up on a portion of the second sidewall bottom surface and the diode set up inside the cavity. Also, Hirano does not show that the first and second patterned conductive reflective films substantially and respectively cover the first and second sidewall of the cavity.




Nevertheless, Tominaga (e.g. fig. 2) shows a light emitting diode package structure having silicon sub mount 11 having a first surface including a cavity 12 including a bottom surface, a first sidewall and a second sidewall wherein a first conductor 13 is set up an a portion of the first surface, bottom surface and first sidewall, a second conductor 13 set up an a portion of the first surface and a second sidewall and a light emitting diode 14 set up in the cavity (pp 0005).




Okazaki teaches that the emission efficiency can be improved by substantially covering the first and second sidewall of the cavity using a first and second metal reflective materials 18/19 (e.g. fig. 6; col. 2/lls. 56-60; col. 4/lls. 60-64).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a cavity having a bottom surface, a first and a second sidewalls in the first surface of the sub mount disclosed by Hirano wherein a first conductor is set up an a portion of the first surface, bottom surface and first sidewall, a second conductor set up an a portion of the first surface and a second sidewall, and a light emitting diode set up in the cavity as suggested by Tominaga to provide a more compact package since the overall thickness is reduced and to make the first and to make the first and second patterned conductive reflective films substantially covering the first and second sidewalls of the cavity as suggested by Okazaki to improve the emission efficiency of the device.

6. Regarding claim 8, Hirano teaches a pair of bumps set up between the first electrode of the light emitting diode and the first patterned conductive reflective film as well as the second electrode of the light emitting diode and the second patterned conductive reflective film.

7. Regarding claim 9, Hirano teaches that the bump comprises Au (col. 11/64-65).

8. Regarding claim 10, Hirano teaches that the package comprises a first and second bonding pads set up on the first and second patterned conductor (e.g. fig. 8A, 9A). With respect to claim language refereeing to the use of the pad such as for connecting electrically with an external circuit board, it is respectfully noted that intended use and/or other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of

performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. *In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963).*

9. Regarding claim 11, Tominaga teaches that an obtuse angle is formed by the bottom surface and the first or second sidewalls.

10. Regarding claim 12, Hirano teaches that the semiconductor sub mount is made of silicon (col. 10/lls. 66-67).

11. Regarding claims 14 and15, Hirano teaches that the semiconductor sub-mount further comprises: a first conductive type semiconductor sub-mount 443 (e.g. n doped or p doped), wherein the first conductive type semiconductor sub-mount has a second conductive type region 441 (e.g. p doped or n doped) therein; and an insulating layer 424 set up on the first conductive type semiconductor sub-mount, wherein one of the electrodes is electrically connected to the second conductive type region but electrically isolated from the first conductive type semiconductor sub-mount through the insulating layer (col. 11/lls. 1-10).

***Response to Arguments***

12. Applicant's arguments have been considered but are persuasive. Regarding applicant's argument that the prior art does not teaches the new added limitations, Hirano teaches that the first conductive pattern 422 directly cover the first conductive type semiconductor substrate whereas the second conductive pattern 421 is separated from the first conductive type semiconductor by the insulating layer 424.

***Conclusion***

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Leonardo Andújar/
Primary Examiner, Art Unit 2826

3/17/2008